Three-Dimensional Packages with Through Silicon Vias: In-situ Stress Characterization and Reliability Assessment

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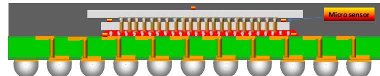
Introduction



Three-dimensional IC stacking is increasingly important to extend silicon technology and to enable "More than Moore," as envisioned by the microelectronics industry. 3D stacks enabled by TSVs have the following advantages:

- Miniaturization
- High bandwidth
- Minimum interconnect latency
- Heterogeneous integration
- Low power consumption
- Potentially low cost

However, relatively less work has addressed the TSV reliability issues. In particular, there is little or no information in open literature on experimental characterization of stresses in wafers with TSVs and stacked dies. This project ***aims to study the reliability of such 3D microelectronic packages with stacked dies using nano-scale and micro-scale sensors and computer simulations.*** The fabrication steps, experimental stress data, and simulation results from this project are important for the development of next-generation microelectronic packages.

TSV Fabrication and Reliability Analysis

- 250-300um silicon substrate
- Double-side process
- No carrier wafer used in the process
- -55ºC to 125ºC
- Fabrication induced defects are analyzed

TSV in Free-Standing Wafer vs. 3D Integrated Package

- In 3D integrated package, global warpage dominates TSV displacement
- Critical locations also shift to microbump region
- Dominating factors affecting TSV/microbump reliability are different in 3D integrated packages and free-standing wafers

In situ Stress Measuring Concept

In situ stress measurements near bump pads are important to help understand the evolution of die stresses associated with the packaging process. Depending on the package, the vias/bumps' pitch ranges from a few microns to a hundred microns.

Desired Features:

- Nano and micron dimensioned resistors
- Low temperature material processes

Figure: Schematic of the resistors in Rosetta configuration about the TSV

Figure: Example nano and microstructures: nano rectangular and triangular looped structures (typical dimensions vary from 50-100 nm wid legs, 300-1000 nm thick), rectangular, triangular and labyrinth looped microstructures (typical dimensions vary from 10-50 μm wide legs, 50-500 μm long, 0.2-1 μm thick).

In Situ Stress Measurement

BULK

Piezoresistance coefficients, elastoresistance coefficients

$$\frac{\Delta\rho_{\alpha\beta}}{\rho}=\sum_{k,l}\pi_{\alpha\beta kl}\sigma_{kl}=\sum_{k,l}\gamma_{\alpha\beta kl}\varepsilon_{kl}$$

$$R=\frac{\rho l}{A}\Rightarrow\frac{\Delta R}{R}=\frac{\Delta\rho}{\rho}+\Delta\left(\frac{l}{A}\right)\frac{A}{l}$$ (GEOMETRY)

$$GF=\frac{\Delta R/R}{\Delta l/l}=\frac{\Delta R}{R\varepsilon}$$

Table: Bulk Material Properties for various material [1][2]

variable	units	NiCr (Nichrome V)	NiCu (Constatan)	Au	Pt	PolySi	Doped Si
Resistance	µohm*cm	108	49	2.44	10.6	n/a	n/a
	ohm*m	1. 08E-06	1.68E-08	2.44E-08	1.06E-07	n/a	n/a
G.F.*	unitless	2.0	2	n/a	4.8	30-40	-100 to 180

Strains Seen on Flip Chip Simulations: ε = 0.000667-0.001667 → for metals ΔR = R(0.0133), need to have R in kΩ to measure ΔR= 120 Ω*

Thin

For metals → Decrease all the dimensions (cross-sectional area & thickness)

*if the thickness is below a micron the resistivity is increased compared to the bulk's by 3-5X's (dependent on processing)

The Scattering Hypothesis:

$$\rho=\rho_0+\rho_{GB}+\rho_{SS}+\rho_{SR}$$

Bulk resistivity, Grain Boundary, Surface Scattering, Roughness

Develop a reliable thin film metallic process of nano resistors with resistances in the kΩ so as to be able to measure resistance change through-out chip assembly.

Figure: (left) Nano-dimensioned thin film resistors with kΩ resistance fabricated using Georgia Tech's state of the art cleanroom facilities

Summary

- Optimized double side process to fabricate TSVs
- Thermal shock reliability testing on the first wafer is in progress from -40C to 125C and already went through 1500 cycles
- In 3D integrated package, critical locations shift to microbump region
- Dominating factors affecting TSV/microbump reliability are different in 3D integrated packages and free-standing wafers
- Metallic thin film resistors offer a solution to help monitor the local stress development around interconnects like TSVs which are:
  - Low Temperature processing
  - Nano to micro-dimensioned resistors

CASPaR — Computer-Aided Simulation of Packaging Reliability

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