Fundamental and Applied Fracture Characterization of Thin Film Systems

Gregory T. Ostrowicki, Nicholas J. Ginga, Sathyav Raghavan, Suresh K. Sitaraman
George W. Woodruff School of Mechanical Engineering | Georgia Institute of Technology

Interlayer Delamination

Problem Statement
Delamination is a reliability concern for microelectronic, photonic, MEMS, and other thin film engineering applications. Quantifying interface strength between films is necessary to predict product life. However, experimentally measuring interface strength between thin films (<100 µm) is challenging. Therefore, new experimental methods are needed to test and measure the bond strength and resistance to delamination between thin film systems.

Magnetically Activated Peel Test (MAPT)
- Three thin film strips attached to a central permanent magnet disc
- Force of magnetic repulsion lifts permanent magnet, and this force is proportional to the voltage supplied to the driving electromagnet
- Thin film-substrate interface strength is determined by mechanical analysis of peeling at the critical load
- Advantages: non-contact, fixtureless, monotonic & fatigue loading, simple and representative fabrication, amenable to environmental conditioning

Test Design

Sample Preparation

Experimental Results

This work is funded by the National Science Foundation under Grant No. CMMI-0800037

Dielectric Cracking

Problem Statement
Micro-scale and nano-scale thin films are being increasingly used in a wide range of emerging technologies including microelectronics, optoelectronics, and MEMS devices. Typically, these thin film layers are composed of many different materials with dissimilar properties. Along with delamination, a common mode of failure for thin films is cohesive fracture, through the thickness of the film. This can be caused by external mechanical loading from handling or dropping the device. CTE mismatch from thermal loading experienced while powering the device. It is desired to characterize and measure the cohesive fracture toughness of these thin films to design devices with better reliability, performance, and life.

Objective
Ongoing research at Georgia Institute of Technology is occurring to develop a fixtureless cohesive fracture toughness test that can be used for nano- and micro-scale thin films.

Advantages
- Test method uses common clean room fabrication techniques
- Capable of small material dimensions (photolithography is the limit)
- The proposed technique does not require fixtureing of the test material or external mechanical loads
- The propose technique has the ability to test a wide range of nanoscale film materials used in microelectronics, photovoltaics, MEMS, medical devices.
- Utilizes a “Super Layer” material to generate and drive fracture

Test Concept

Main Idea - Use intrinsic stress of Super Layer to generate fracture in films below it. Crack propagation will cease when the energy supplied by the super layer is equal to the critical fracture energy of the test material, and therefore provide a measurement of the fracture toughness of the test material.

Preliminary Results

Test Material: SiO₂
  Thickness = 1.2 µm
  Stress = 1.2 GPa
  Au Release layer
  Thickness = 200 nm

Test Material: SiO₂
  Thickness = 230 nm
  Stress = 1.2 GPa
  Au Release layer
  Thickness = 230 nm

Applied Package Cracking

Problem Statement
During Pb free flip-chip assembly, the stresses between a silicon chip and an multi layered organic substrate are so high that a fracture in the interlayer dielectric (ILD) in the vicinity of the solder bump may occur.

Objectives
- To characterize interfacial and cohesive crack propagation in nanoscale BEoL stacks.
- To device an effective criterion for crack propagation through multilayered structures.

Approach
- Global – local modeling approach was used to model the nanoscale BEoL stacks.
- A global assembly of the flip chip was modeled in ANSYS.
- In the current approach a crack of known length is embedded into the stack (local model) and strain energy release rate (G) is determined using virtual crack closure technique.

Local Model and Results

Global Model Results

Local models with embedded interfacial and cohesive cracks in the BEoL stack was developed. Cracks were simulated to propagate towards the chip center and the change in G with respect to the crack length was studied.

Acknowledgements

This work is funded by the National Science Foundation under Grant No. CMMI-0800037

Interfacial Crack Propagation

Cohesive Crack Propagation

The curves indicate that there is a sudden change in G near the copper traces.