Mechanically Compliant Single-Path and Multi-Path Electrical Interconnects

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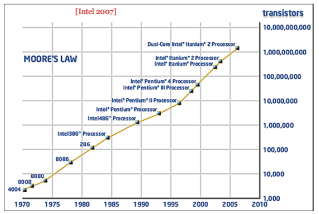
Background

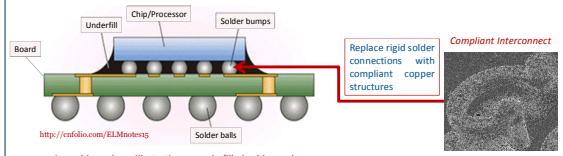
Moore's law states that the number of transistors on a chip will double approximately every two years.



Processor development timeline illustrating Moore's law

Microprocessor development has followed this trend leading to more communications with-in a given chip size.

To accommodate the increased communications between the chip and motherboard, Input/Output (I/O) port sizes on the chip continue to be scaled down to increase their count over a given chip area.



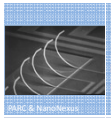
Assembly package illustrating an underfilled solder package

For high performance chips, solder balls have typically been the interconnection of choice linking the chip's I/Os with the mother-board's. However, due to the scale down in size of the I/Os and solder balls, coupled with the coefficient of thermal expansion mismatch between the chip and motherboard, solder balls by themselves can no longer reliably attach the chip to the board. Hence prompting the development of new technology, *compliant interconnects*.

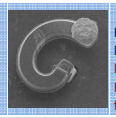
Research Objectives

- Enhance mechanical compliance
  - 7 mm/N to reduce die stresses/prevent low-k cracking
  - Improve Copper interconnect fatigue live to ~1000 cycles
- Improved electrical performance
  - Lower electrical resistance
  - Lower self and mutual Inductance
- Cost effective solution
  - Batch fabrication
  - Reduced number of fabrication steps
  - Compatible with current industry practices
- Vibration Analysis
  - Understand behavior of Compliant Interconnect assemblies under Shock and Impact loads

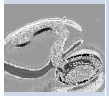
Highlights of Select Designs



J-Springs [Ma et al, 2002]
Ultra-fine density
High compliance
Non-standard fab process
High contact resistance

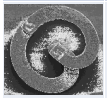


G-Helix [Zhu et al, 2004]
High Compliance
Batch Fabrication
High electrical parasitics
Moderately costly fabrication



Sea of Leads [Bakir et al, '03]
No underfill
Batch Fabrication
Limited compliance
Electroplated gold

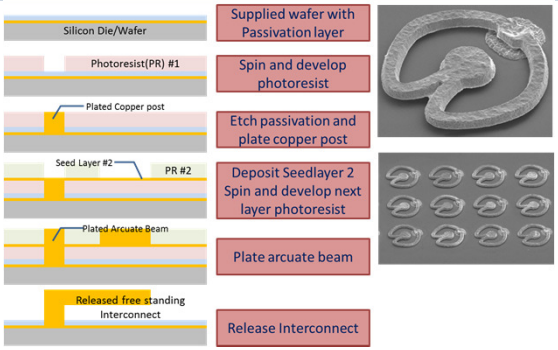
ELASTec [Dudek et al, 2006]
No underfill
Batch fabrication
Limited Compliance
Limited Pitch



Beta-Helix [Zhu et al, 2004]
High compliance
Batch Fabrication
Costly fabrication
High electrical parasitics

Flex Connect [Kacker, 2008]
High compliance
Good electrical parasitics
Relatively low cost fabrication

Fabrication



Performance Comparison

Fatigue life characterization of interconnects is based on a Coffin-Manson type equation using plastic strain range as failure metric.

$$N_f^{-0.6} \times \varepsilon_f^{0.75} = \Delta\varepsilon_p$$

*Coefficients are representative for annealed copper
ε_f – fatigue ductility coefficient; $\Delta\varepsilon_p$ – plastic strain range; N_f – fatigue life

Failure in all cases was observed in the copper interconnect structures. These packages were not underfilled by design.

	Resistance [m-Ohm]	Inductance [pH]	Compliance [mm/N]	Fatigue life [cycles]
J-Springs	∞	NA	10000	NA
Sea of Lead	NA	NA	0.91	NA
Beta Helix	51.4	102	11.1	>3000
G-Helix	42.7	92.7	11.5	3118
Flex	40.9	36.5	6.47	~1000
Multi-path	37	37	~3	>1000

Impact Analysis: Board-Level Drop Test

- Board-level drop test simulation was conducted to understand response under Impact loading
- Simulation results for board deflection agree with published data and analytical calculation
- This approach will be extended to Impact Testing of Compliant Interconnects and validated against experimental data

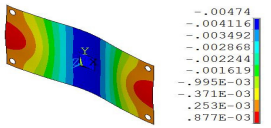
Comparison of Deflection Results

	Deflection (mm)	Stress ,SX (MPa)	Strain (μstrain)
Input G simulation	5.21864	355.956	21738.6
Analytical Calculation	5.1579	357	22300
Error (%)	1.1639	0.2932	2.5825

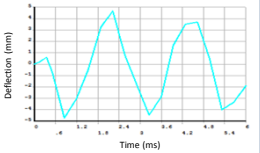
Converting Acceleration to Displacement (Input-G Method):

$$d(t) = \int_0^t \int_0^\tau G(\tau)\, d\tau\, d\tau$$

$$d(t) = \int_0^t G(\tau)\, d\tau = \int_0^t G_m \tau\, d\tau = \frac{1}{2} G_m t^2$$

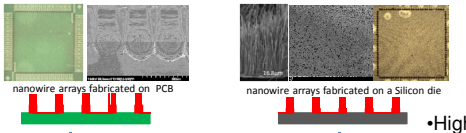


Deflection Contour Plot

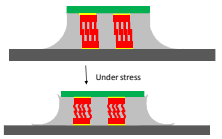


Deflection of Board Center

Compliant Nanowire Z-axis Interconnect

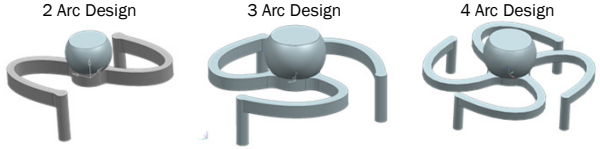


- Very strong bond between Nanowires & substrate
- Highly compliant due to the very high aspect ratio of the nanowires,



- Low temperature assembly is possible due to the depressed melting-point of nanowires
- "Velcro-like" bonding has larger contact surface compared to planar contact
- Solder free assemblies are possible.

Multi-path Designs



Multi-path Compliant Interconnects

- Design targeted at obtaining suitable compromise between electrical and mechanical properties
- Symmetric design allows for uniform in plane compliance
- Multi-path also diminishes effects of electrical parasitics
- Domed variation may find use for probing applications
- May also find application as micro-vibration absorbers

CASPaR
Computer Aided Simulation of Package Reliability

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