Electroplated Compliant Off-Chip Interconnects

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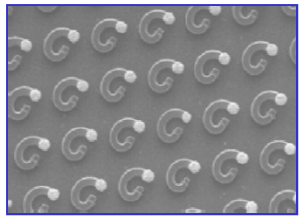
OBJECTIVES and APPROACH

- ❑ Design, model and optimize a novel complaint Helix interconnect for fine pitch applications to meet ITRS requirements for Year 2016 and beyond
- ❑ Determine the necessary compliance to accommodate the differential displacement due to CTE mismatch and to exert minimal force on die pads for low-K/Cu dies
- ❑ Ensure that the induced cyclic stress/strain in the interconnects will not be high enough to produce early fatigue failures
- ❑Model and determine the electrical characteristics of the interconnect at different frequencies
- ❑ Customize interconnect geometry based on distance from center of die to maximize electrical performance and ensure sufficient reliability
- ❑ Fabricate and assemble dies with helix interconnects on organic substrates and assess reliability through thermal cycling

IMPACT and BENEFITS

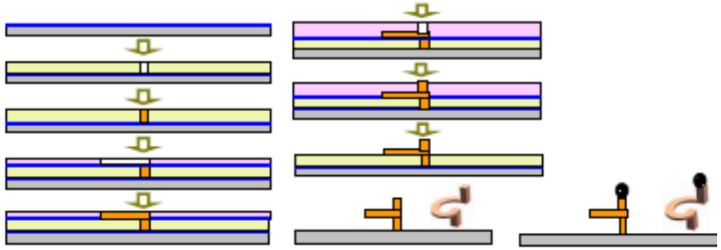
- ❑ Lead-free wafer level interconnects to meet the industry requirements for the next 10 years
- ❑ No underfill required; reworkable interconnects
- ❑ High Compliance; compatible with low-K/copper dies
- ❑ Utilizes standard IC fabrication processes, wafer scale and batch fabrication; potentially cost-effective
- ❑ Scalable with pitch



SEM Pictures of Compliant Helix Interconnect

ACCOMPLISHMENTS

- ❑ Characterized and optimized structure for mechanical and electrical performance
- ❑ Fabricated helix interconnects at a 100 micron pitch using lithography and electroplating processes
- ❑ Assembled 20mm x 20mm die at a 100 micron pitch on organic substrates without underfill
- ❑ Assemblies thermal cycled from 0°C to 100°C, interconnects last in excess of a 1000 thermal cycles; more testing is needed
- ❑ Simulations show that interconnects introduce minimal interfacial stress at die/interconnect interface



Fabrication Process

FUTURE WORK

- ❑ Modify the process so that the interconnects can be fabricated in two or fewer masking steps
- ❑ Assemble and test a heterogeneous array of interconnects such that the central ones are column-like and outer ones are helix-like; will use the same masking steps.
- ❑ Perform electrical characterization of the compliant interconnects
- ❑ Variations of our compliant interconnects are being pursued by semiconductor industry for potential future applications.